ANDOR DESIGN CORP

CPCI301
MIL-STD-1553 A, B & McAir
MULTI PROTOCOLS
Simulator/Analyzer/Tester

CPCI BUS Interface Card

FEATURES

*** SUPPORTS VALIDATION/PRODUCTION TEST PLANS.**
*** SIMULTANEOUS BC, MULTIPLE RTS, MONITOR.**
*** 1553A. B, McAir AND USER DEFINED PROTOCOLS.**
*** 16/32 BIT TIME TAG.**
*** FULL ERROR DETECTION AND GENERATION.**
*** ON BOARD MAJOR/MINOR FRAME TIMING.**
*** PROGRAMMABLE MESSAGE PARAMETERS.**
*** PROGRAMMABLE OUTPUT AMPLITUDE.**
*** SOFTWARE WITH SOURCE CODE INCLUDED.**
*** AUTO INCREMENTING MEMORY STORAGE**
*** 128K x 16 DUAL PORT STATIC RAM.**

DEVICE TYPE

Size CPCI 3U size
Type 32 Bits, 5 Volts, Target only.

DESCRIPTION

The CPCI301 is a full-featured, high performance, Dual Redundant MIL-STD-1553 serial bus Simulator Analyzer Tester designed as a plug in card for a CPCI backplane. The CPCI301 includes full error injection and can operate in independent or simultaneous mode as a Bus Controller, multiple simulated Remote Terminals and full/selective Monitor. Its data structure can be changed on the fly without interrupting the processor for real time operation. The active monitor stores, time tag and annotates bus traffic with the message type and any detected errors. Stored words are annotated with a break down of the word error.

APPLICATIONS

The CPCI301 can be used for Validation Testing, Production Testing, full bus simulation and monitoring, as a general purpose 1553 interface or a stand alone bus Analyzer. For precise message scheduling and measurements, the Major and minor frame times are independent of message sequences or retransmissions on errors and the start of all command messages are independent of message length, response time or length of response. Message timing is calibrated and RT responses have low jitter.

GENERAL	SPECIFICATIONS
Parameter	Value
1553 SRAM	128K x 16
Major Frame Count	1 to 32768, Continuous
Major Frame Size	1 to 1024 Minor Frames
Minor Frame Time	0 to 419 msec.
Minor Frame Size	0 to 32766 Commands
BC Messages	0 to 2048
Message intervals	2 to 6400 usec. in .1 sec. steps
Response Timeout	2 to 33 usec. in .5 usec. steps
Response Time	2 to 33 usec. in .5 usec. steps
Response jitter	50ns Max
Retry on Error	Same or alternate bus
Internal time tag	16/32 bits
	1, 6.4 or 64 usec. steps

WORD ERROR INJECTION/DETECTION
- Low bit count (1, 2)
- High bit count (1, 2, 3)
- Parity error
- Manchester low
- Manchester high
- Inverted Sync
- Zero crossing deviation (+/- 150 nsec, External)

MESSAGE ERROR INJECTION/DETECTION
- Format
- Response/Late response
- Sync
- Non contiguous data (2 usec.)
- Word count error
- Data on two channels
- Status word
- Invalid Word

MAXIMUM RATINGS	
Parameter	Value
Temperature Range	
Operating	0 to +70 Deg. C
Storage	-65 to +150 Deg. C
*Power supplies	
+5 Volts +/- 5%	0.4 Amps Max
+12 Volts +/- 5%	0.100 Amps 50% duty cycle
Physical characteristics	
3U Size CPCI card	

SOFTWARE
The CPCI301 comes with software drivers for DOS and Windows 98/NT/2000/XP. A set of well documented API's with Source code written in "C" is included.

STAND ALONE OPERATION
A menu driven user interface is included for stand-alone operation. With this program the user can set up 1553 traffic, simulate RT'S responses, monitor all or selected traffic in real time and capture data using trigger and search arguments.

DATA FILTERING
The CPCI301 data filter looks at the complete command rather than just addresses and sub addresses. Individual Messages are designated to be ignored, monitored, replied to or monitored and replied to.

CPCI301 OPERATION
The CPCI301 processes 1553 messages with a minimum attention from the CPU. The user need only write a set of command Blocks, a message list and number of messages to define a minor frame of 1553 messages. He writes a minor frame time, the number of minor frames per major frame and a minor frame list to define a major frame. The bus controller sends the major frame a number of times as programmed in the major frame count, without any further attention from the CPU.

In the Remote Terminal mode, the user writes a set of command Blocks and a look-up table for the CPCI301 to respond autonomously to incoming messages. In both modes an active monitor analyzes, annotates and stores bus traffic in a monitor Buffer.

The CPCI301 generates ten interrupt flags to show completion of a frame in the BC mode, receipt of a specified message, receipt of a specified Data word, receipt of a specified Status word, detected message errors or triggers.

1553 OUTPUT
- Direct coupling
- Transformer stub coupling

COMPUTER INTERFACE
The PIC301 operates as a 32 bits, target-only device with interrupt support. An auto indexing Dual ported, static RAM serves as the intermediate for data exchange between the on board CPCI FIFO and the 1553 bus. An auto incrementing address register serves to hold the initial RAM Address and increments after each data transfer. Two additional registers control the mode of operation.

Both the registers and the RAM can be loaded with new data while a message is being transmitted over the 1553 channel for real time applications. Essentially, programming the CPCI301 consists of transferring data to or from the RAM and the host.

For specialized features or unique interface requirements, please contact the factory.

Specifications subject to change without notice.

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